WHAT IS CLAIMED IS:

1. A system for facilitating inter-processor communication in a multiple processor computer system having one or more shared resources, comprising:

a first mailbox associated with a first processor for indicating the status of the shared resources in the system and for sharing one or more tasks among the multiple processors;

a second mailbox associated with a second processor for indicating the status of the shared resources in the system and for sharing one or more tasks among the multiple processors; and

a semaphore unit for indicating the status of the shared resources in the system and for notifying the first and second processors of a particular task to be executed by the respective processors.

2. The system of Claim 1, wherein the first processor is a host processor and the second processor is a co-processor.

3. The system of Claim 1, wherein the tasks are shared among the multiple processors without latency.

4. The system of Claim 1, wherein either the first or second mailbox receives a message from the semaphore unit indicating a task to be executed, and wherein the first or second mailbox notifies its associated processor of the message.

5. The system of Claim 4, wherein either the first or second mailbox causes a respective interrupt signal to be communicated to its associated processor when a message is received from the semaphore unit.

6. The system of Claim 5, wherein, in response to the respective interrupt signal, the associated processor services the interrupt signal by reading the message from the associated mailbox.

7. The system of Claim 6, wherein upon reading the message from the associated mailbox, the mailbox is cleared and an acknowledge notification is communicated by the mailbox to the other processor to indicate that the mailbox is empty and that the task is being executed.

8. The system of Claim 1, wherein the semaphore unit comprises a first plurality of semaphore registers for indicating the status of a shared resource in the system and a second plurality of semaphore registers for indicating messages that are communicated to the first and second mailboxes to notify a respective processor of a task to be executed.

9. The system of Claim 8, wherein the semaphore registers are controlled by a semaphore controller.

10. The system of Claim 8, wherein the first plurality of semaphore registers comprises a first register for indicating the status of a shared resource in the system, a second register for setting particular bits in the first register to indicate the data stored in a particular memory location of the shared resource, and a third register for clearing particular bits in the first register.

11. The system of Claim 10, wherein the first, second, and third registers are 32 bit registers.

12. The system of Claim 10, wherein the first register comprises a first bit portion wherein each individual bit is associated with a particular shared resource in the system, and a second bit portion for indicating the data stored in a particular memory location of that particular shared resource.

13. The system of Claim 12, wherein the first bit portion comprises six bits such that the most significant bit in the first bit portion is associated with a host instruction memory, the next most significant bit in the first bit portion is associated with a ping buffer, the next most significant bit in the first bit portion is associated with a pong buffer, the next most significant bit in the first bit portion is associated with a coprocessor instruction memory, the next most significant bit in the first bit portion is associated with a cache memory, and the least significant bit in the first bit portion is associated with input/output resources.

14. The system of Claim 12, wherein in response to being notified of a task to be executed, the respective processor reads the data from the first register to execute the task.

15. The system of Claim 8, wherein the second plurality of registers comprises a fourth register and a fifth register each for indicating a message for the respective mailboxes of a task to be executed.

16. A system for facilitating inter-processor communication in a multiple processor computer system having one or more shared resources, comprising:

means for cooperatively multitasking and preemptively multitasking among the multiple processors;

means for notifying a respective processor of a particular task to be executed;

means for indicating the status of the shared resources in the system; and

means for communicating the status of a particular shared resource to the processor for execution of the task.

17. A method for facilitating inter-processor communication in a multiple processor computer system having one or more shared resources, comprising the steps of:

sending a message to a first mailbox indicating a task to be executed by a first processor;

notifying the first processor of the message;

reading the message from the first mailbox;

configuring a first semaphore register to indicate the data contained at a desired address location of a particular one of the shared resources; and

accessing the first semaphore register and reading the data from the first semaphore register to execute the task.

18. The method of Claim 17, wherein the notifying step comprises the step of interrupting the first processor with an interrupt signal.

19. The method of Claim 17, wherein upon performing the reading step further performing the step of clearing the message from the first mailbox and sending an acknowledge message to a second processor informing the second processor that the first mailbox is empty and that the task is being performed.

20. The method of Claim 17, further comprising the step of clearing the data in the first semaphore register.